WE CLAIM:

1. A circuit for analog-to-digital conversion, comprising:

a first pre-amplification circuit, comprising a plurality of amplifiers;

a second pre-amplification circuit, comprising a plurality of amplifiers, that is coupled to the first pre-amplification circuit; and

a series of adjustment resistors coupled between each of the first series of nodes and an input of each of the amplifiers of the second pre-amplification circuit.

2. The circuit of Claim 1, further comprising a series of averaging resistors coupled between an output of each amplifier of the first pre-amplification circuit at a first series of nodes.

3. The circuit of Claim 1, further comprising at least one additional pre-amplification circuit comprising a plurality of amplifiers and one additional associated series of averaging resistors coupled between an output of each amplifier of the additional pre-amplification circuit.

4. The circuit of Claim 3, further comprising at least one additional series of adjustment resistors coupled to an input of each amplifier of the additional pre-amplification circuit.

5. The circuit of Claim 4, wherein each pre-amplification circuit is configured to receive an adjustment current.

6. The circuit of Claim 5, wherein the adjustment current is determined during a calibration of the analog-to-digital conversion circuit by varying the adjustment current such that an effect of total offset error for each pre-amplification circuit is substantially minimized.

7. The circuit of Claim 6, wherein the calibration is performed during at least one of when the circuit is first powered on and when an operating temperature of the analog-to-digital conversion circuit exceeds a predetermined threshold.

8. The circuit of Claim 1, further comprising a series of interpolation resistors coupled between an output of each amplifier of the second pre-amplification circuit at a second series of nodes, wherein at least one of an averaging and an interpolation resistor is coupled between outputs of any two amplifiers, and wherein the second series of nodes are coupled to an input of a comparator in a comparator circuit at a predetermined ratio.

9. The circuit of Claim 8, wherein the predetermined ratio of amplifier outputs to comparator inputs is three to one.

10. A circuit for analog-to-digital conversion, comprising:

a first pre-amplification circuit, comprising a plurality of amplifiers;

a second pre-amplification circuit, comprising a plurality of amplifiers, that is coupled to the first pre-amplification circuit; and

a series of adjustment resistors coupled between each of the first series of nodes and an input of each of the amplifiers of the second pre-amplification circuit.

11. The circuit of Claim 10, further comprising:

a series of averaging resistors coupled between an output of each amplifier of the first pre-amplification circuit at a first series of nodes; and

a series of averaging resistors coupled between an output of each amplifier of the second pre-amplification circuit at a second series of nodes.

12. The circuit of Claim 10, further comprising:

a comparator circuit comprising a plurality of comparators, wherein an input of each comparator is coupled to a node in the second series of nodes.

13. The circuit of Claim 11, further comprising at least one additional pre-amplification circuit, comprising a plurality of amplifiers, that is coupled between the first and second pre-amplification circuits and one additional associated series of averaging resistors between an output of each amplifier of the additional pre-amplification circuit.

14. The circuit of Claim 13, further comprising at least one additional series of adjustment resistors coupled to the inputs of the at least one additional pre-amplification circuit.

15. The circuit of Claim 11, wherein the adjustment current is determined during a calibration of the analog-to-digital conversion circuit by varying the adjustment current such that an effect of total offset error for each pre-amplification circuit is substantially minimized.

16. The circuit of Claim 11, wherein a number of amplifiers in the pre-amplification circuit is determined by a desired resolution of an output digital signal.

17. The circuit of Claim 11, wherein the amplifiers comprise transistor pairs, each of the respective transistor pairs further comprising a respective current source driving the pair.

18. The circuit of Claim 17, wherein the transistor pairs further comprise at least one of a BJT transistor pair, a FET transistor pair, and a CMOS transistor pair.

19. A method for improving linearity of an analog-to-digital conversion circuit, the method comprising:

providing an adjustment current, during a calibration of the analog-to-digital conversion circuit, to each amplifier in a pre-amplification circuit through an adjustment resistor coupled to an input of each amplifier; and

determining a value of the adjustment current, such that an effect of offset error in an output of each pre-amplification circuit is substantially minimized.

20. The method of Claim 19, wherein the adjustment current comprises one of a single-ended current and a differential current.

21. A method for determining a digital value of an analog signal, the method comprising:

receiving an analog signal through an input of an amplifier in a first pre-amplification circuit;

subjecting the analog signal to an averaging process and an adjustment process, wherein:

the averaging process is performed by a series of averaging resistors connecting outputs of the amplifiers of the first pre-amplification circuit, and

the adjustment process is performed by injecting an adjustment current into an adjustment resistor connecting an output of an amplifier of the first pre-amplification circuit to an input of an amplifier of a second pre-amplification circuit; and

performing a comparison on the pre-amplified analog signal in a comparator circuit that is coupled to the second pre-amplification circuit.

22. The method of Claim 21, wherein a value of the adjustment current is determined during a calibration process such that an effect of offset error of the pre-amplification circuits is substantially minimized.

23. The method of Claim 21, wherein the calibration process is performed during at least one of when the pre-amplification circuits are first powered on and when an operating temperature of the pre-amplification circuits exceeds a predetermined threshold.

24. A circuit with an analog-to-digital conversion architecture, comprising:

means for providing a first pre-amplification comprising a plurality of amplifying means;

means for providing a second pre-amplification with a folding analog-to-digital converter architecture comprising a plurality of amplifying means;

means for providing averaging between outputs of each amplifying means in the first pre-amplification means at a first series of nodes;

means for providing an adjustment between the first series of nodes and an input of each of the amplifying means of the second pre-amplification means; and

means for comparing to convert analog signal to digital signal, coupled to an output of the second pre-amplification means.